AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A method for accessing a FIFO memory from a CPU comprising:

receiving ~~a plurality of requests~~one read or write request from the CPU, ~~each of the plurality of requests~~ the read or write request specifying an address;

determining if ~~an~~the address ~~corresponding with one of the plurality of requests~~ is within a range of multiple addresses; and

causing ~~a~~the FIFO memory to be accessed whenever ~~an~~the address ~~corresponding with a request~~ is within the range of multiple addresses, the FIFO memory being identified by and accessible only through a single address, ~~whereby~~and reading from or writing to the FIFO memory ~~is accessed using any one of the addresses in the range of multiple addresses~~a plurality of times through the single address in response to the one read or write request from the CPU.

2-4. (Cancelled)

5. (Currently amended) An apparatus comprising:

a FIFO memory identified by and accessible only through a single address; and

at least one unit ~~to receive a plurality of requests~~that

receives one read or write request from a CPU, ~~each of the plurality of requests~~ the read or write request specifying an address,

~~to~~ determines if ~~an~~the address ~~corresponding with one of the plurality of requests~~ is within a range of multiple addresses, and

~~to~~ causes the FIFO memory to be accessed whenever ~~an~~the address ~~corresponding with a request~~ is within the range of multiple addresses, ~~whereby the memory is accessed using any one of the addresses in the range of multiple addresses~~and

reads from or writes to the FIFO memory a plurality of times through the single address in response to the one read or write request fro the CPU.

6-8. (Cancelled)

9. (Currently amended) A medium readable by a machine embodying a program of instructions executable by the machine to perform a method for accessing a FIFO memory from a CPU, the method comprising the steps of:

receiving ~~a plurality of requests~~one read or write request from the CPU, ~~each of the plurality of requests~~ the read or write request specifying an address;

determining if ~~an~~the address ~~corresponding with one of the plurality of requests~~ is within a range of multiple addresses; and

causing ~~a~~the FIFO memory to be accessed whenever ~~an~~the address ~~corresponding with a request~~ is within the range of multiple addresses, the FIFO memory being identified by and accessible only through a single address, ~~whereby~~and reading from or writing to the FIFO memory ~~is accessed using any one of the addresses in the range of multiple addresses~~a plurality of times through the single address in response to the one read or write request from the CPU.

10-12. (Cancelled)

13. (Currently amended) A system for burst mode data transfers, comprising:

a bus;

a ~~processor~~CPU, coupled with the bus to place a plurality of requests on the bus, each of the plurality of requests specifying an address;

a FIFO memory, coupled with the bus, the memory being identified by and accessible only through a single address; and

at least one unit, coupled with the bus and with the FIFO memory ~~to receive a plurality of requests~~that

receives one read or write request from a CPU, ~~each of the plurality of requests~~ the read or write request specifying an address,

~~to~~ determines if ~~an~~the address ~~corresponding with one of the plurality of requests~~ is within a range of multiple addresses, and

~~to~~ causes the FIFO memory to be accessed whenever ~~an~~the address ~~corresponding with a request~~ is within the range of multiple addresses, ~~whereby the memory is accessed using any one of the addresses in the range of multiple addresses~~and

reads from or writes to the FIFO memory a plurality of times through the single address in response to the one read or write request fro the CPU.

14-20. (Cancelled)